## ABSTRACT OF THE DISCLOSURE

Architecture for a cache fabricated on a die with a processor including a plurality of cache banks, each containing a plurality of memory cell sub arrays. The sub arrays including a plurality of arrays of memory cells, the arrays including regular arrays and at least one redundant sub array. Logic circuitry is associated with each cache bank. A change in a single bit of the logic circuitry from a first to a second logic state causes one of the regular arrays to become disconnected from the global data bus, and the redundant array to become connected to the global data bus.